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TRANSFORMERLESS SWITCHED-CAPACITOR INVERTER WITH REDUCED NUMBER OF SWITCHING COMPONENTS FOR PV APPLICATION

Kasinath Jena
School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India
Email- kasi.jena@gmail.com

Chinmoya Kumar Panigrahi
School of Electrical Engineering, KIIT Deemed to be University, Bhubaneswar, India

Krishna Kumar Gupta
THAPAR University, Patiala, India

Abstract
A novel transformerless switched-capacitor (SC) inverter with minimum part count and reduced voltage stresses is proposed in this paper. The suggested inverter generates a five-level waveform using nine switches, two capacitors, and a diode. Design description, working principle, and control techniques are described in detail. Some of the most remarkable properties of the proposed architecture are its ability to increase the input voltage while keeping zero leakage current and its self-balancing capabilities of the capacitors. A comparison to prior-art topologies demonstrates the suggested topology benefits. Lastly, a laboratory prototype has been built to check its feasibility and effectiveness.
Keywords-Transformerless inverter, leakage current, component count per level.

摘要
本文提出了一种具有最少部件数和降低电压应力的新型无变压器开关电容器 (SC) 逆变器。 建议的逆变器使用九个开关、两个电容器和一个二极管生成五电平波形。 详细介绍了设计说明、工作原理和控制技术。 所提出的架构的一些最显着的特性是它能够在保持零泄漏电流的同时增加输入电压和电容器的自平衡能力。 与现有技术拓扑的比较展示了建议的拓扑优势。 最后，建立了一个实验室原型来检查其可行性和有效性。
关键词-无变压器逆变器、漏电流、每级元件数。

1.Introduction

Nowadays, Photovoltaic power generation gains significant advantages due to easy applicability, improved performance, low cost, environmental and social acceptability. A power converter serves as a link between a photovoltaic (PV) system and the grid. [1]-[2].

In practice, the grid-connected PV inverter is of two types, viz. transformer-based and transformer-less inverter. The key advantages of using a transformer-based inverter are galvanic

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About the authors: Kasinath Jena
Corresponding author- kasi.jena@gmail.com

separation between the grid and the PV module, eliminating leakage current, and ensuring both humans and the system's safety. Alternatively, the inclusion of a transformer makes the inverter more expensive, bulkier, and less efficient than it otherwise would be. A transformer-less inverter can overcome the drawbacks of a transformer-based inverter. On the other hand, transformerless inverters are susceptible to leakage current, ground fault, electromagnetic effect, and increased losses. There are worries about safety due to the lack of galvanic separation between the solar photovoltaic panel and the electrical grid [3-11].

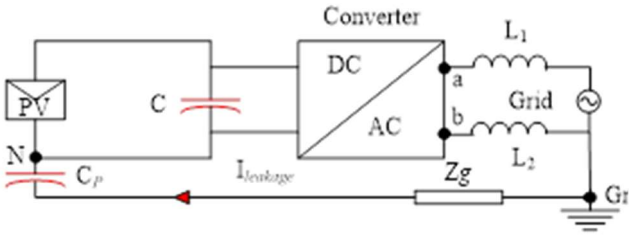


Fig.1 Typical transformerless topology

FIig.1 depicts the equivalent circuit diagram of a typical transformer-less inverter [26] in its simplified form. It composes semiconductor switches, output filter, parasitic capacitance, and ground impedance. On the other hand, variations in common-mode voltage result in a significant leakage current in the PV system, which flows via the parasitic capacitor C_P of the PV modules. Therefore, the total common-mode voltage defined by [22]

$$v_{cm} = \frac{(v_{aN}+v_{bN})}{2} \quad (1)$$

$$v_{dm} = (v_{aN} - v_{bN})\left(\frac{L_2-L_1}{2(L_1+L_2)}\right) \quad (2)$$

Total common-mode voltage (v_{tcm}) can be represented as

$$v_{tcm} = \frac{(v_{aN}+v_{bN})}{2} + (v_{aN} - v_{bN})\left(\frac{L_2-L_1}{2(L_1+L_2)}\right) \quad (3)$$

And leakage current can be written as

$$I_{leakage} = C_P \frac{d(v_{tcm})}{dt} \quad (4)$$

Concerning point N, the potential differences between points a and b are denoted by the variables v_{aN}, v_{bN}.

v_{cm}, v_{dm} be the common-mode voltage and differential voltage, respectively.

In a transformerless inverter, however, two distinct ways can limit or eliminate leakage current. These approaches are commonly known as the modified PWM technique [3-5] and structurally designed [6-21]. According to the structural design, three strategies are implemented to mitigate or suppress the leakage current. These approaches are classified as

(a) Neutral point clamped technique

(b) Decoupling of DC/ AC side technique.

(c) Common ground technique.

The neutral point clamped topologies for PV application, presented in [6-10] to minimalize or suppress leakage current. The topology suggested in [6] utilized the full DC bus voltage but lacks boosting ability. Additionally, the topologies [7-10] require a DC-link voltage twice the grid voltage peak value and a larger percentage of switching components.

Decoupling of DC/AC side of a transformer-less inverter is suggested in [11-15]. However, all the topologies are based on a full-bridge structure and isolate the grid from the PV module during the zero states to prevent leakage current. But the leakage current in these topologies is not wholly suppressed or eliminated. Moreover, it requires a more significant number of switching components to suppress the leakage current, making it costly, complex, and unreliable.

The issues of the above two methods can be overcome by using the common ground configuration technique suggested in [16-21] [26]. The PV module's negative terminal is

connected directly to the utility grid neutral point in this configuration, and capacitors generate negative polarity voltages. The main disadvantages of the following topologies are that they have more active and passive parts, which makes it more challenging to limit leakage current.

A revolutionary single-source five-level common ground transformer-less switched-capacitor (SC) topology has been developed in this novel work, and it has the following distinct properties

(a) The ability to increase the voltage level of the output voltage.
(b) Eliminate the leakage current.
(c) Self-balancing property of the capacitor.
(d) Least number of switching components
(e) Lower voltage stress
(f) Utilization of a single DC source

2. PROPOSED TOPOLOGY

2.1 Circuit description

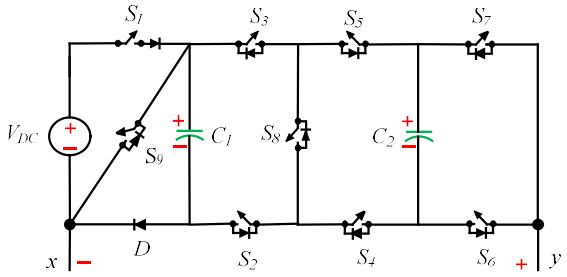


Fig.1. Common ground five-level transformer less SC topology

The proposed schematic diagram is depicted in Fig. 1. It composes nine power switches (S_1, S_2 ..S_9), one power diode (D), two capacitors (C_1, C_2,) and a single DC source (V_{DC}). Every switch consists of one transistor with an anti-parallel diode (IGBTs) except switch S_1. The switch S_1 comprises a transistor with a series-connected diode. Due to the PV panel's direct connection to the grid neutral point, no parasitic capacitance exists between the PV panel and the ground. As a result, the leakage current is negligible. The topology can synthesize five levels at its output ($\pm 2V_{DC}$, $\pm 1V_{DC}$, and 0). All switches have a maximum inverse (PIV) voltage that is limited to the supply voltage. The coordinates x and y denote the load terminals. $V_{xy}(t)$, i_{xy}(t) denote the voltage and current of the load, respectively. The switching combination for the different valid voltage levels is tabulated in Table I. The symbols " ↑ " and " ↓ " indicate that capacitors are being charged or discharged, respectively. The dotted lines in red and green represent the direction of the load current and the charging path of the capacitor.

TABLE I.VALID SWITCHING COMBINATION FOR DIFFERENT MODES OF OPERATION

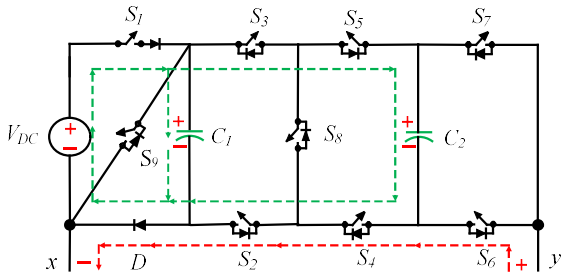
Mode	Active switch	$V_{xy}(t)$	Effect of capacitor
1	S_1, S_2, S_3, S_4, S_5, S_6	0	$C_1\uparrow$, $C_2\uparrow$
2	S_1, S_2, S_3, S_4, S_5, S_7	$+1V_{DC}$	$C_1\uparrow$, $C_2\uparrow$
	S_1, S_2, S_5, S_6, S_8	$-1V_{DC}$	$C_1\uparrow$, $C_2\downarrow$
3	S_1, S_3, S_4, S_7, S_8	$+2V_{DC}$	$C_1\uparrow$, $C_2\downarrow$
	S_2, S_5, S_4, S_6, S_9	$-2V_{DC}$	$C_1\downarrow$, $C_2\downarrow$

2.2 Principle operation

The following modes illustrate the operational principle.

mode.1 $V_{xy}(t) = 0$

when S_1, S_2, S_3, S_4, S_5, S_6 are turned on, the voltage across the load $V_{xy}(t) = 0$. Capacitors C_1, C_2 gets charged to V_{DC}. Load current flows through the path V_{DC}-S_1-S_3-S_5-C_2-S_6-$LOAD$-V_{DC} shown in Fig.2 (a).



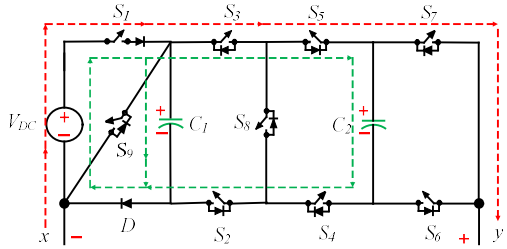
(a)

Fig.2.(a) $V_{xy}(t) = 0$

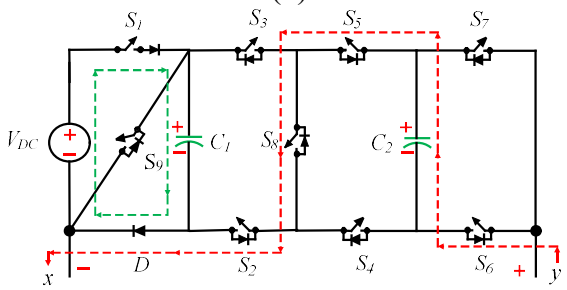
- mode 2. $V_{xy}(t) = \pm V_{DC}$

when S_2, S_3, S_4, S_5, S_7 are turned on, the voltage across the load $V_{xy}(t) = +V_{DC}$. Capacitors C_1 and C_2 gets charged up to a voltage source V_{DC}. Load current flows through the path V_{DC}-S_1-S_3-S_5-S_7-*LOAD*-V_{DC} shown in Fig.2(b).

When S_1, S_2, S_5, S_6, S_8 are turned on, the voltage across the load $V_{xy}(t) = -V_{DC}$. The capacitor C_1 gets charged up to V_{DC} and capacitor C_2 releases its stored energy to the load. The load current path through S_6-C_2-S_5-S_8-S_2-*D*-*load*-S_6 is shown in Fig.2 (c).



(b)



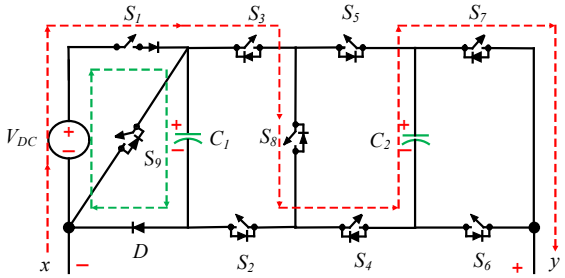
(c)

Fig.2.(b) $V_{xy}(t) = +V_{DC}$ (c) $V_{xy}(t) = -V_{DC}$

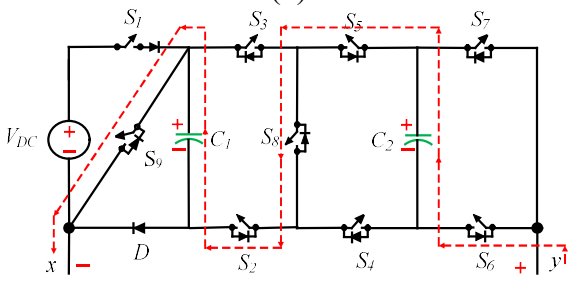
- Mode 3. $V_{xy}(t) = \pm 2V_{DC}$

when S_1, S_3, S_4, S_7, S_8 are turned on, the voltage across the load $V_{xy}(t) = +2V_{DC}$. The capacitor C_1 gets charged up to a voltage source V_{DC} and C_2 releases its stored energy to the load along with the supply. Load current flows through the path V_{DC}-S_1-S_3-S_8-S_4-S_6-C_2-S_7-*LOAD*-V_{DC} shown in Fig.2(d).

When S_2, S_5, S_4, S_6, S_9 are turned on, the voltage across the load is $V_{xy}(t) = -2V_{DC}$. Both the capacitors C_1, C_2 releases their stored energy to the load through the path S_6-C_2-S_5-S_8-S_2-C_1-S_9-*LOAD*-S_6 shown in Fig.2(e).



(d)



(d)

Fig.2.(C) $V_{xy}(t) = +2V_{DC}$ (D) $V_{xy}(t) = -2V_{DC}$

2.3 Selection of capacitor

The rating of the capacitors is appropriately chosen for the inverter design because the capacitor's ripple voltage will affect the system efficiency and the physical size of the capacitors, which makes the inverter bulky and costly. Therefore, optimum values of capacitance are selected to limit the voltage ripple and physical size. The optimum values of capacitance depend upon the acceptable voltage ripples and discharging values of the capacitor. The capacitor's discharging values are dependent on

the following factors: the maximum load current, the longest discharging period, and the power factor angle. Hence, the discharging quantity of charge (ΔQ_{ci}) of the capacitors is given by the equation (5)

$$\Delta Q_{ci}=\int_{t_a}^{t_b} I_{max.}\sin(\omega t-\emptyset)\,d\omega t \qquad (5)$$

Where $I_{max.}$: maximum values of load current

$\emptyset$: power factor angle

(t_a, t_b): discharging period.

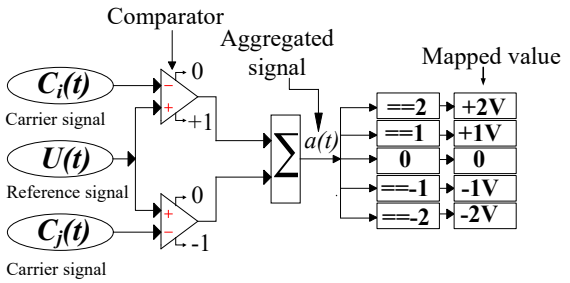
Thus, the optimal capacitance values must satisfy the following criteria. [23]

$$C_i \geq \frac{\Delta Q_{Ci}}{\Delta V_{Ci}} \qquad (6)$$

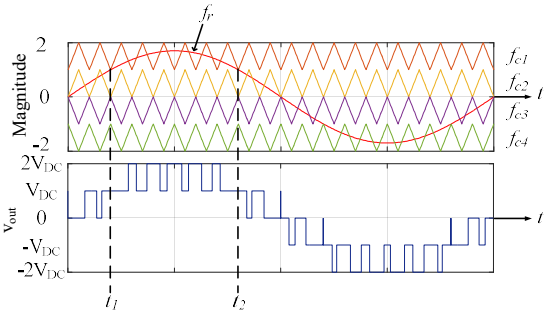
Where ΔV_{Ci}= is the voltage ripple of the capacitor.

3. MODULATION STRATEGY

Switching techniques can be divided into two fundamental categories: low switching frequency switching techniques and high switching frequency switching techniques. The proposed topology utilized a simple logic-based multicarrier PWM approach [25]. The modulation technique is illustrated in Figure 3. (a). In this approach, a 50 Hz sinusoidal wave with a modulation index (M) of 0.95 is used as the reference signal U(t). Four triangular waves with the same amplitude and frequency (2KHz) are considered to be the carrier signals above and below the reference axis: $C_i(t)$ (i=1,2) and $C_j(t)$ (j=3,4)}. The aggregate signal is obtained by continuously comparing sinusoidal signals to carrier signals. Following that, switching pulses are generated by comparing the aggregated signal to the mapped values followed by a constant, as illustrated in Figure 3. (a).



(a)



(b)

Fig.3 (a) Modulation scheme (b) Reference & carrier signal, output voltage.

4. POWER LOSSES ANALYSIS

There are three sorts of losses that occur in this proposed topology. These losses are classified as follows: (a) switching losses; (b) conduction losses. (c) Losses due to voltage ripples.

4.1. Switching losses

Switching operation causes switching losses [24]

The following is an expression for switching losses during turn-on:

$$P_{on,sw} = \frac{1}{6} f_0 (V_{on} I_{on} t_{on}) \qquad (14)$$

During turn off:

$$P_{off,sw} = \frac{1}{6} f_0 (V_{off} I_{off} t_{off}) \qquad (15)$$

Where, V_{on}, V_{off} : voltage across switches before and after they are turned on.

I_{on}, I_{off}be : Current flowing through switches immediately following their activation and just before to their deactivation.

t_{on} and t_{off} : The switch turn-on and turn-off times.

Thus, the proposed topology overall switching power losses (P_{sw}) are stated in equation (16)

$P_{sw} = \sum_{l=1}^{5}\sum_{m=1}^{9}\left(P_{on,sw,m} + P_{off,sw,m}\right)$ (16)

Where l and m denote the level and switch counts, respectively.

4.2 Conduction losses (P_{con})

The conduction losses arise as a result of the power switches being in the on-state condition. Henceforth, the overall conduction losses are the summation of power losses of the power switch and diode [25].

$P_{con}=V_{s,on,m}I_{s,avg,m} + I_{s,rms,m}^2 R_{s,on,m} + V_{d,on,m}I_{d,avg,m} + I_{d,rms,m}^2 R_{d,on,m}$ (17)

The voltages applied to the switch and diode when in the on position is represented by $V_{s,on,m}, V_{d.on,m}$. The average and maximum currents of the switch and diode are $I_{s,avg,m}, I_{d,avg,m}$ and $I_{s,rms,m}, I_{d,rms,m}$ respectively.

4.3 Capacitor ripple losses (P_R)

The charging current of the capacitor causes voltage ripple. This voltage ripple can be illustrated as [23]

TABLE III. COMPARATIVE ANALYSIS WITH THE LATEST SWITCHED CAPACITOR TRANSFORMERLESS TOPOLOGY

Ref.	N_L	N_S	N_{SW}	N_C	N_D	O	$F_{C/L}$	G
[6]	5	1	7	3	2	-	2.6	1
[9]	4	1	4	4	2	-	2.75	1.5
[10]	5	1	6	3	-	-	2	0.5
[15]	5	1	8	4	6	-	3.8	0.5
[17]	3	1	5	2	-	-	2.6	1
[18]	5	1	6	3	1	1	2.4	1
[26]	5	1	8	3	-	-	2.4	1
[19]	3	1	5	2	-	-	2.66	1
[21]	3	1	4	2	1	-	2.66	1
[P]	5	1	9	2	1	-	2.6	2
O:other components, G: gain								

$F_{C/L}=\frac{N_S+N_{SW}+N_D+N_C+N_O}{N_L}$ (22)

Where N_L: Number of levels, N_C: Number of capacitors, N_D: Number of diodes, N_{Sw}: Number of semiconductor switches; N_S: Number of DC sources, N_O: Number of other components. The $F_{C/L}$ factor determines the cost, weight, and size of the inverter, as well as its efficiency. The switches play an important role since they are related to the driver unit, heat sink, protection unit, and other components, all of which raise the weight, size, volume, and cost of the product. Table III shows that the topologies [10][15] generate five levels of voltage, even though they cannot raise the voltage. Additionally, topology [15] has a higher proportion of switching components, which helps to reduce leakage current. Topologies [6] [9] [17] [19] [21] utilize a more significant number of switching components to create the desired voltage levels and have a lower gain than the proposed design. However, the topologies [26] [18] have fewer active and passive elements per level but do not have any boosting ability.

$\Delta V_{C_i}=\frac{1}{C_i}\int_{t_a}^{t_b} I_c(t)dt$ (18)

Where $\Delta V_C, I_c(t)$ be the ripple voltage and maximum charging current, respectively. t_a and t_b are the longest discharging period.

Thus, the ripple loss can be stated as follows:

Ripple loss $(P_{R.}) = \frac{f_0}{2}\sum_{i=1}^{2}(C_i \Delta V_{Ci}^2)$ (19)

Therefore, the total losses (P_T) can be expressed as

$P_T = P_{sw} + P_c + P_R$ (20)

So the overall efficiency (η)

$\eta = \left(\frac{P_{out}}{P_{out}+P_T}\right) \times 100$ (21)

5. COMPARATIVE STUDY

Table III compares the proposed topology with the recent topologies to its merits. It is primarily concerned with the following factors: component count per level and boosting ability. The characteristic, Component per level ($F_{C/L}$) can be expressed as

6. SIMULATION AND EXPERIMENTAL OUTCOMES

6.1 Simulation outcomes

The proposed topology theoretical analysis has been validated using the MATLAB/Simulink

environment. Table IV contains the specified simulation settings parameters. Fig. 4(a-b) shows the simulation outcomes. It has been seen that when the load voltage reaches its maximum magnitude, it is two times the supply voltage. However, despite a sudden change in load, the magnitude of the load voltage does not change significantly. The voltages across the capacitors are depicted in Fig. 4(c-d), which maintained a voltage of about 100V under load-changing circumstances.

TABLE II. Parameters for simulation and experimental setup

Parameter	Specification
DC source (V_{DC})	50V
Output frequency (f_0)	50Hz
switching frequency	100Hz,2KHz
RL-Load	R=50Ω,L=120mH
Capacitors (C_1=C_2)	4700μF
Power Switches	MOSFET
Modulation index (M)	0.95

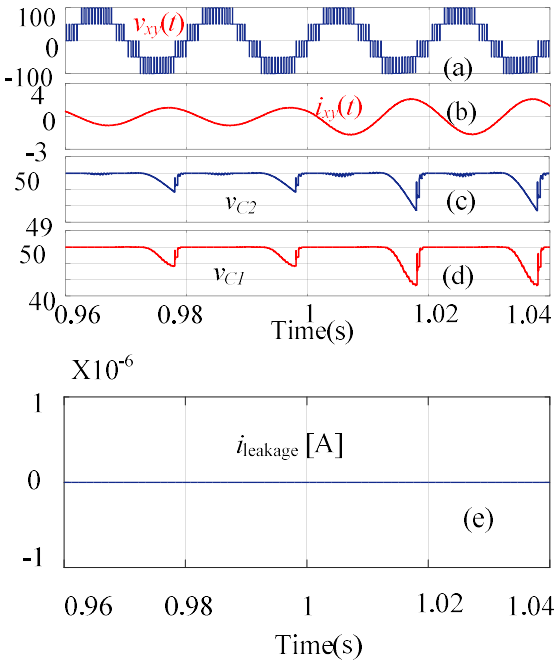


Fig.5. For R-L and R- Load (a) voltage (b) current (c) voltage across C_1 (d) voltage across C_2 (e) leakage current

6.2 Experimental results

A hardware prototype of the proposed topology has been created to validate the simulation results. The parameters that have been used for the experimental setup are listed in Table II.

An inverter must be tolerant to changes in operating conditions to provide great performance. As a result, dynamic test results are included here

(a) change in switching frequency:

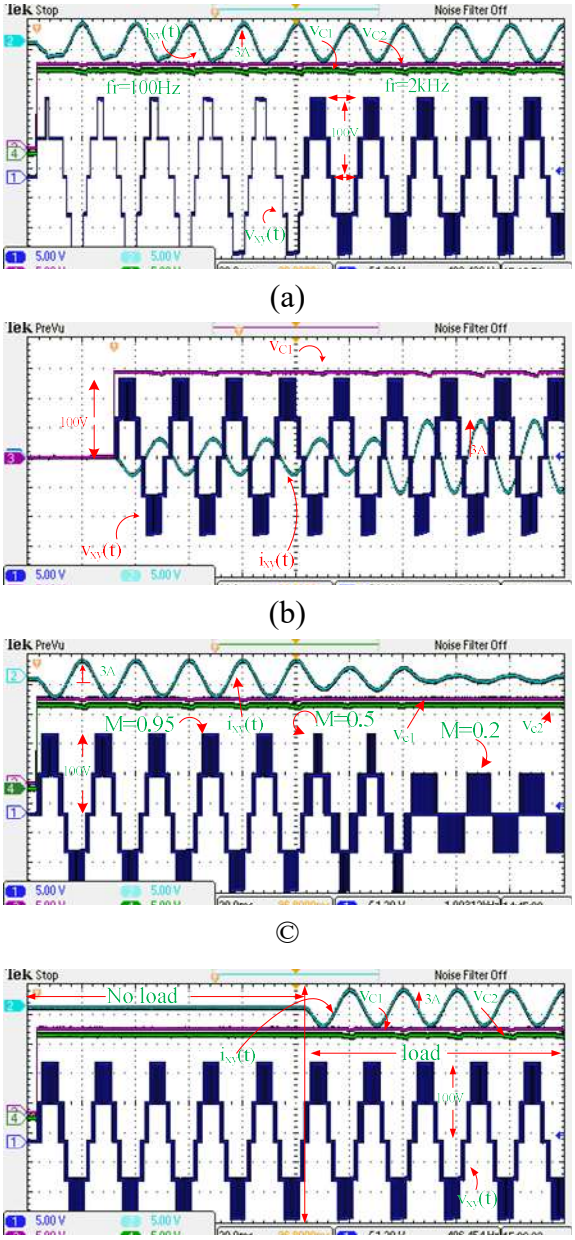
When the switching frequency varies, the proposed inverter can adjust appropriately.Fig.5(a) illustrates the output voltage and current as a function of frequency. in these circumstances (100 Hz to 2000Hz), the inverter responds quickly.

(b) Change in load:

Fig.5(b) depicts the experimental findings when the load is suddenly changed. The load change is set as follows: from no load to resistive-inductive load (30 & 15mH). The results demonstrate that the inverter functions admirably under changing load conditions.

© Change in modulation index:

Fig.5(c) illustrates the load voltage when the modulation wave's amplitude varies. As illustrated in Fig.5(c), when M is changed from 0.9 to 0.6, then to 0.2, its output voltage decreases from five to five levels and finally to three. The transient procedures are completed quickly, demonstrating the suggested inverter high dynamic performance. Steady-state results are shown in Fig.5(d). It confirms that the unique work generates five-level and capacitors are retaining their self-balancing property.



(a)

(b)

©

(d)

Fig.6. Experimental outcomes (a) change in switching frequency (b) change in load (b) change in modulation index (d) steady-state results.

7. CONCLUSION

This paper demonstrates a common ground SC transformerless topology, eliminating the leakage current and enhancing the load voltage. In particular, minimal leakage current, a minimum amount of switching components per level, reduced voltage stress, and the self-balancing property of capacitors voltage are the key advantages of this design. The enhancement of voltage boosting ability is more competent for the renewable energy source. Testing results indicate that the inverter performs well under varying conditions.

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